Thomas J. Nijssen

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Objective

Motivated Computer Engineer finishing up a Computer Engineering M.S. degree looking for a full-time position in digital hardware design, computer architecture, systems design and programming, or verification.

Education

University of California, Santa Cruz – GPA 3.71 *2015 – 2021*

Master of Science in Computer Engineering (expected graduation: June 2021)

Bachelor of Science in Computer Engineering; Minor in Electrical Engineering (earned June 2019)

Masters Thesis: Identifying and de-duplicating reuse of hardware module instantiation in the ESSENT logic simulator to reduce compile times and executable size.

Selected Coursework:

- Distributed Systems
- Compiler Design
- Programming Languages
- Advanced Parallel Processing
- Computer Architecture
- Programmable Hardware Accelerators
- Introduction to Operating Systems
- Microprocessor System Design
- Logic Design

Skills

Programming Languages: SystemVerilog, Perl, Python, C, C#, C++, Scala, Java, Tcl, Erlang, Chisel, FIRRTL, SQL.

Tools: Xilinx Vivado, Cadence OrCAD, Synopsys Synplify Pro, Verilator, Yosys Open Synthesis Suite.

Architectures: RISC-V, OpenRISC, Universal Flash Storage.

Miscellaneous: Linux administration, Git, parallel processing.

Experience

Teradyne, Inc. *Hardware Engineering Intern, Summer 2020, 2019*

- Verified proper operation and standards-compliance of a commercial UFS protocol tester. Implemented new functionality requested by customers.
- Researched alternatives to existing synthesis workflow to speed up turnaround time and ensure timing closure.

Baskin School of Engineering, UCSC *Teaching Assistant & Lab Tutor, March 2017 – June 2020*

- Mentored over 60 introductory logic design students each quarter by discussing and helping to debug their designs.
- Assisted 40 undergraduate computer architecture students through weekly interactive discussion sections guided by custom-designed handouts.
- Commended by students for clarity and helpfulness and a patient, practical, reassuring approach; praised by instructors for paying close attention to student needs and identifying common misunderstandings.

Faculty Instructional Technology Center, UCSC *Student Consultant, March 2016 – June 2019*

- Supported and instructed over 100 faculty members in their use of the Canvas Learning Management System.
- Orchestrated the automated archival of over 2TB of faculty materials from a legacy platform.

Broadcom Wireless Systems Division *Test Engineering Intern, Summer 2018, 2017*

- Implemented new testing framework using National Instruments PXIe devices to achieve a 100x speedup and greatly increased reliability.
- Redesigned probe card to test multiple parts simultaneously and improve fault tolerance.

Achronix Semiconductor Corporation *Research & Development Intern, Summer 2012*

- Researched feasibility of including OpenRISC 1200 and OpenSPARC as a small core within larger designs.
- Ported the existing vendor-specific primitives to use the Achronix-specific block RAMs.

Selected Projects

SlugSat – UCSC's first cubesat project *2018 – 2019*

- Designed On-Board Computer using STM32 microcontroller to control HF linear transponder.
- Mentored colleagues in embedded programming skills, especially in using a RTOS.

RISC-V 5-stage in-order processor *May 2018*

- Implemented the RV32I/64I subset in Verilog.
- Simulated using Verilator, running Dhrystone as a testbench.
- Synthesized using Yosys to explore design resource usage.