THOMAS J. NIJSSEN

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Objective

I am a motivated Computer Engineering student pursuing a Computer Engineering M.S. degree and am looking to gain experience in digital hardware design through internships in the fields of computer architecture, design reuse, and verification.

Education

University of California, Santa Cruz Santa Cruz, CA

Computer Engineering, M.S. (expected graduation: June 2021)

Computer Engineering, B.S.; Minor in Electrical Engineering (earned June 2019)

Selected Coursework: Advanced Parallel Processing, Computer Architecture, Programmable Hardware Accelerators, Microprocessor System Design, Introduction to Operating Systems, Logic Design.

Skills

Programming Languages: *Proficient:* Verilog, Perl, Python, C, C#, C++, Java, Tcl. *Intermediate:* Matlab, Chisel.

Frameworks & Tools: Xilinx Vivado, Microchip MPLAB X. Cadence OrCAD, Synopsys Synplify Pro, RISC-V, OpenRISC, FIRRTL, Verilator Simulation Tool, Yosys Open Synthesis Suite, Universal Flash Storage.

Experience

Graduate Researcher September 2019 – Present

Vertical Architectures, Memories, and Algorithms Group, UCSC Santa Cruz, CA

- Leverage FIRRTL to design a fast simulator generator that leverages novel partitioning algorithms.
- Implementing essential features such as VCD (waveform) dumping.

Logic Design Teaching Assistant & Lab Tutor March 2017 – Present

Baskin School of Engineering, UCSC Santa Cruz, CA

- Mentor students by discussing their approach to their assignments and debugging their designs.
- Commended by students for clarity and helpfulness and a patient, practical approach that maximizes students' understanding.

Hardware Engineering Intern June 2019 – September 2019

Teradyne, Inc. San Jose, CA

- Verified proper operation and standards-compliance of commercial UFS protocol tester.
- Researched alternatives to existing synthesis workflow to speed up turnaround time and ensure timing closure.

Student Consultant March 2016 – June 2019

Faculty Instructional Technology Center, UCSC Santa Cruz, CA

- Supported and instructed faculty with their use of the Learning Management System.
- Orchestrated the automated archival of faculty materials from a legacy system.

Test Engineering Intern June 2017 – September 2018

Broadcom Wireless Systems Division San Jose, CA

- Implemented testing framework using National Instruments PXIe devices to achieve a 100x speedup and greatly increased reliability.
- Redesigned probe card to test multiple parts simultaneously and improve fault tolerance.

Research & Development Intern August 2012

Achronix Semiconductor Corporation San Jose, CA

- Researched feasibility of including OpenRISC 1200 and OpenSPARC as a small core within larger designs.
- Ported the memories within OpenRISC to use the Achronix-specific block RAMs.

Selected Projects

SlugSat – UCSC's first cubesat project 2018 – 2019

- Designed On-Board Computer using STM32 microcontrollers to control HF linear transponder.
- Mentored colleagues in embedded programming particularities, especially in using a RTOS.

RISC-V 5-stage in-order processor May 2018

- Implemented the RV32I/64I subset in Verilog.
- Simulated using Verilator, running Dhrystone as a testbench.
- Synthesized using Yosys to optimize design.